UNITED STATES PATENT AND TRADEMARK OFFICE

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10/717,335	11/19/2003	Joichi Bita	3408.68745	8257

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EXAMINER
DILLON, SAMUEL A

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>05 June 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-16</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>19 November 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   The Examiner acknowledges the applicant's submission of the amendment dated
June 5, 2006. Per the amendment, <u>Claims 1-2, 4, 6-10, 12 and 15-16</u> been amended.

2.   The instant application having Application No. 10/717,335 has a total of 16
claims pending in the application; there are 2 independent claims and 14 dependent
claims, all of which are ready for examination by the examiner.

I. <u>RESPONSE TO AMENDMENT(S) / ARGUMENT(S)</u>

3.   In response to the amendment, the <u>objections to the Claims</u> as stated in the
previous action are **withdrawn**.

4.   In response to the amendment, the <u>35 U.S.C. 112 second paragraph rejections
of Claims 1-16</u> as stated in the previous action are **withdrawn**.

35 U.S.C. 103 Rejections – Hubis and Kitamura

5.   The Applicant's arguments with respect to the **35 U.S.C. 103 rejections of
Claims 1-2, 4, 7, 9-10 and 15** have been fully considered and are **not persuasive**.

6.   <u>The Applicant contends that neither Hubis nor Kitamura disclose acquiring a
storage page of the mirror area in another controller by referring to the table</u> *(Remarks,
paragraph 2)*. More specifically, the Applicant contends that Hubis fails to disclose the
mirror management table and acquisition of a storage page of the mirror area in another
controller by referring to the table, and that Kitamura fails to disclose acquiring a storage

page of the mirror area in another controller by referring to the table *(Remarks,*
paragraph 5).

The Examiner notes that the Applicant has amended <u>Claims 1 and 9</u> to read *"a*
mirror management table for (...) managing allocation of a storage page in a/the mirror
area of said second cache memory", and also notes that the Applicant remarks that
"Kitamura discloses a mirror management for allocation of a storage page in the mirror
area of another controller" (Remarks, paragraph 5). Accordingly, it is interpreted that the
limitation the Applicant contends Hubis and Kitamura do not disclose is the *"acquiring a*
storage page... by referring to the table".

Kitamura discloses a system manager registering content items to be mirrored
through interaction with the mirror management tool *(column 14 lines 20-27)* and the
mirror management control program then performing the mirroring operation by referring
to the mirror management table *(column 14 lines 4-5)*. Accordingly, Kitamura does
disclose acquiring a storage page of the mirror area in another controller by referring to
the table.

7.   <u>The Applicant also contends that Hubis does not disclose a node channel for</u>
<u>direct communications</u> *(Remarks, paragraph 5)*. More specifically, the Applicant
contends Hubis does not fulfill the limitation *"a node channel circuit for performing direct*
communication between said control units".

The limitation "node channel circuit" is interpreted claiming a circuit having a
channel of communication between nodes, where a channel can be interpreted as a
physical connection. Hubis discloses a controller copying data to the mirror cache of the

other controller over the backend bus using a special mirror cache write command.

Accordingly, Hubis does disclose a node channel circuit for performing direct

communication between said control units.

35 U.S.C. 103 Rejections – H&K in view of Tam, Beardsley, Rowson, Li

8.   The Applicant's arguments with respect to the **35 U.S.C. 103 rejections of**

Claims 3, 5-6, 8, 11, 13-14 and 16 have been fully considered and are **not persuasive**.

The Examiner notes that the sole rationale put forth by the Applicant regarding the

allowability of said claims is their dependence on claims contended to be allowable. The

Applicant is directed to the argument traversal of Claims 1-2, 4, 7, 9-10 and 15 above.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103 – Hubis and Kitamura

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

10.   **Claims 1-2, 4, 7, 9-10, 12 and 15** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hubis *(US Patent Number 6,321,298)* in view of Kitamura et al. *(US*

Patent Number 6,247,012).

11.   As per **Claim 1**, Hubis discloses a storage control apparatus *(figure 1)* for

accessing a storage device *(shared storage devices 108)* according to a data access

request *(host write command 128, column 3 lines 49-50)* from a requesting apparatus

(host computer 1, figure 1), comprising:

a first controller *(RAID controller 1, figure 1)* which has a first cache memory

(cache 112-1, figure 1) and is in charge *(via bus 110, figure 1, see below)* of a first

storage device *(any of shared storage devices 108)* out of a plurality of storage devices

(shared storage devices 108); and

a second controller *(RAID controller 2)* which has a second cache memory

(cache 112-2, figure 1) and is in charge *(via bus 110, figure 1, see below)* of a second

storage device *(any of shared storage devices 108)* out of said plurality of storage

devices, and

a mirror area *(write mirror cache 118-2, figure 2)* of said second cache memory,

and a mirror area *(write mirror cache 118-1, figure 2)* of said first cache memory,

and wherein when said first controller receives a data write request *(host write*

command 128, column 3 lines 49-50) containing write data from said requesting

apparatus, said first controller allocates a page *(destination in first controller, see below)*

in a read/write area *(write cache 116-1, figure 2)* of said first cache memory, acquires a

storage page *(subset of mirror area, see below)* in the mirror area of said second cache

memory, writes *(transfer 107-1, figure 2)* the write data *(write data 138, column 3 line*

51) from said requesting apparatus to the page allocated in the read/write area of said

first cache memory, and copies *(column 3 lines 55-58)* the write data to the acquired

page in the mirror area of said second cache memory.

The Examiner notes that inherent in writing data to the read/write area in the first controller is the data being written to a subset of the read/write area, where a subset is either the entirety or a part of the read/write area. Subsequently, this subset fulfills the limitation "a page in a read/write area" cited on page 23 line 19. It is also inherent in copying the data to the mirror area of the second controller that the data is written to a subset of the mirror area, and this subset fulfills the limitation "a storage page in the mirror area" cited on page 23 line 20.

Hubis does not expressly disclose said first controller further comprising a first mirror management table for managing allocation of a storage page in a mirror area of said second cache memory, and said second controller further comprising a second mirror management table for managing allocation of a storage page in a mirror area of said first cache memory.

Kitamura discloses a mirror management table *(mirror management table 35, figure 12)* for managing a mirror area *(back-up copy of the primary data, column 2 lines 37-38)* of a memory *(secondary data storage system, column 2 lines 36-37)*.

Hubis and Kitamura are analogous art in that they both deal with managing the mirroring of data in distinct locations.

At the time of the invention it would have been obvious to a person ordinary skill in the art to use Kitamura's mirror management table to manage the cache mirroring taught by Hubis .

The motivation for doing so would have been the ease of managing the storage locations in the memory's mirror. Kitamura discloses that mirror management permits

the system to register content items to be mirrored, mirroring conditions and the storage

location of an archive *(column 14 lines 21-25)*.

Therefore, it would have been obvious to combine Kitamura's mirror

management table with the cache mirroring of Hubis for the benefit of managing storage

locations to obtain the invention as specified in claim 1.

12.   As per **Claim 2**, <u>Hubis</u> and <u>Kitamura</u> disclose the storage control apparatus

according to claim 1, wherein said first and second controllers mutually notify the sizes

of said first and second cache memories *(see below)*, allocate the mirror areas of said

first and second cache memories according to the sizes of said first and second cache

memories *(see below)*, and create said first and second mirror management tables from

said allocation *(Kitamura, column 14 lines 20-25)*.

The concept of mirroring of a region of memory inherently involves recreating all

contents of the region, including size. As per the interpretation made in paragraph 12 of

this office action, the allocation of the mirror areas according to the sizes of the cache

memories is then inherent in the device taught by Hubis *(Hubis, figure 2)*.

13.   As per **Claim 4**, <u>Hubis</u> and <u>Kitamura</u> disclose the storage control apparatus

according to claim 1, wherein when said first controller is degraded *(Hubis, "failure of

controller", column 1 lines 38-41)*, said second controller takes charge of the storage

apparatus which said first controller is in charge of *(Hubis, column 1 lines 45-48)*, and

links the copy page in the mirror area of said second cache memory to said read/write

area *(Hubis, column 1 lines 45-48)*.

14.   As per **Claim 7**, Hubis and Kitamura disclose the storage control apparatus

according to claim 1, wherein each one of said first and second controllers comprises:

        a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory

and said storage device; and

        a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing

direct communication between said control units.

15.   As per **Claim 9**, Hubis and Kitamura disclose a storage control method for

accessing a storage device *(Hubis, shared storage devices 108)* according to a data

access request *(Hubis, host write command 128, column 3 lines 49-50)* containing write

data from a requesting apparatus *(Hubis, host computer 1, figure 1)*, comprising the

steps of:

        allocating a page *(Hubis, subset of read/write area, see rejection of claim 1)* in a

read/write area *(Hubis, write cache 116-1, figure 2)* of a first cache memory *(Hubis,*

cache 112-1, figure 1) disposed in one controller *(Hubis, RAID controller 1, figure 1)* of a

pair of controllers *(Hubis, RAID controllers 1 and 2, figure 1)* when said one controller

receives a data write request *(Hubis, host write command 128, column 3 lines 49-50)*

from said requesting apparatus;

        acquiring a storage page *(Hubis, subset of mirror area, see rejection of claim 1)*

in a mirror area *(Hubis, write mirror cache 118-2, figure 2)* of a second cache memory

(Hubis, cache 112-2, figure 1) referring to a first mirror management table *(Kitamura,*

mirror management table 35, figure 12) which is disposed in said one controller for

managing allocation of a storage page in the mirror area of said second cache memory

of said other controller;

writing *(Hubis, transfer 107-1, figure 2)* the write data *(Hubis, write data 138,*

column 3 line 51) from said requesting apparatus to the page allocated in the read/write

area of said first cache memory; and

copying *(Hubis, column 3 lines 55-58)* the write data to the acquired page in the

mirror area of said second cache memory after said writing.

16.   As per **Claim 10**, Hubis and Kitamura disclose the storage control method

according to claim 9, further comprising the steps of: mutually notifying the sizes of said

first and second cache memories between both controllers *(see below)*; allocating the

mirror areas of said first and second cache memories according to the sizes of said first

and second cache memories *(see below)*; and creating said first and second mirror

management tables from said allocation *(Kitamura, column 14 lines 20-25)*.

The concept of mirroring of a region of memory inherently involves recreating all

contents of the region, including size. As per the interpretation made in paragraph 18 of

this office action, the allocation of the mirror areas according to the sizes of the cache

memories is then inherent in the device taught by Hubis *(Hubis, figure 2)*.

17.   As per **Claim 12**, Hubis and Kitamura disclose the storage control method

according to claim 9, further comprising a step of taking charge *(Hubis, column 1 lines*

45-48) of the storage device which said one controller is in charge of by said other

controller when said one controller is degraded *(Hubis, "failure of controller", column 1*

lines 38-41), and linking the storage page in the mirror area of said second cache

memory to the read/write area of the second cache memory *(Hubis, column 1 lines 45-48)*.

18.   As per **Claim 15**, Hubis and Kitamura disclose the storage control method

according to claim 9, wherein each one of said pair of controllers comprises

a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory

and said storage apparatus, and

a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing

direct communication between said control units.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Tam

19.   **Claims 3 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number*

6,247,012) as applied to claims 1 and 9 respectively above, in further view of Tam et al.

("A Taxonomy-Based Comparison of Several Distributed Shared Memory Systems").

20.   As per **Claim 3**, Hubis and Kitamura disclose the storage control apparatus

according to claim 1, wherein said first controller writes *(Hubis, column 3 lines 50-51)*

back the data, which is written in the page allocated in the read/write area of said first

cache memory *(Hubis, column 3 lines 50-52)*, to said storage device.

Hubis and Kitamura do not disclose the storage control apparatus then releasing

said acquired page of said first mirror management table.

Tam discloses releasing *("pass back the page", section 2.1.3, lines 8-9)* said

acquired page *(page, section 2 paragraph 3 line 1)* of said first mirror management

table.

Hubis, Kitamura and Tam are analogous art in that they deal with maintaining

coherency in shared memory systems.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to have the write procedure between caches of Hubis and Kitamura lock

the pages they access, as per the teachings of Tam.

The motivation for doing so would have been making sure the caches are

synchronized, something Hubis is concerned with *(column 1 lines 49-51)*. Tam

discloses that a cache coherence protocol is needed to ensure that caches always read

a valid copy of a page *(section 1.2, line 11-12)*.

Therefore, it would have been obvious to combine Hubis and Kitamura's caches

with Tam's cache coherence protocol for the benefit of ensuring caches always read

valid copies of pages to obtain the invention as specified in claim 3.

21.   As per **Claim 11**, Hubis, Kitamura and Tam disclose the storage control method

according to claim 9, further comprising the steps of:

writing back *(Hubis, column 3 lines 50-51)* the data, which is written in the page

allocated in the read/write area of said first cache memory *(Hubis, column 3 lines 50-*

52), to said storage device; and

releasing *(Tam, "pass back the page", section 2.1.3, lines 8-9)* said acquired

page *(Tam, page, section 2 paragraph 3 line 1)* of said first mirror management table

when said write back completes.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Beardsley

22.   **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number*

6,247,012) as applied to claims 4 and 12 respectively above, in further view of

Beardsley et al. *(US Patent Number 6,304,980)*.

23.   As per **Claim 5**, Hubis and Kitamura disclose the storage control apparatus

according to claim 4. Hubis and Kitamura do not disclose wherein said second controller

disables read/write processing to the mirror area of said second cache memory.

Beardsley discloses said second controller disabling *(step 945, figure 9)*

read/write processing to the mirror area of said second cache memory.

The primary controller in Hubis accesses *(column 1 lines 37-38)* the mirror area

of the second controller on the basis of write operations issued by a host *(host 102,*

column 1 line 17). Beardsley discloses issuing a stop command to host applications to

stop input/output to the primary device *(step 945, figure 9)*, which effectively stops

processing by the primary controller.

Hubis, Kitamura and Beardsley are analogous art in that they deal with storage

controllers maintaining access to data during controller failures.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to modify Hubis and Kitamura's secondary controller to issue a stop

command to applications communicating with the primary controller in the case of a

failure, as taught by Beardsley.

Beardsley teaches that the motivation for doing so would have been to maintain

data integrity during several types of primary and secondary subsystem errors *(column*

8, lines 39-41).

Therefore, it would have been obvious to combine Hubis' controllers with

Beardsley's application stop command for the benefit of maintaining data integrity to

obtain the invention as specified in claim 5.

24.   As per **Claim 13**, Hubis, Kitamura and Beardsley disclose the storage control

method according to claim 12, further comprising a step of disabling *(Beardsley, step*

945, figure 9) read/write processing to the mirror area of said second cache memory.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Rowson

25.   **Claims 6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number*

6,,247,012) as applied to claim 1 and 9 respectively above, in further view of Rowson

("Interface-Based Design").

26.   As per **Claim 6**, Hubis and Kitamura disclose the storage control apparatus

according to claim 1, wherein when said first controller receives a data write request for

a page from said requesting apparatus, said first controller allocates a page in the

read/write area of said first cache memory, acquires a storage page in the mirror area of said second cache memory referring to said first mirror management table, writes the write data from said requesting apparatus to the allocated page in the read/write area of said first cache memory, and copies the write data to the acquired page in the mirror area of said second cache memory.

Hubis and Kitamura do not disclose the page instead being a plurality of pages, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying.

Rowson discloses a data write request for a plurality of pages *(write-burst, section 5 paragraph 6 lines 1-3)*, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying *(section 5, paragraph 7 lines 1-4)*.

Hubis, Kitamura and Rowson are analogous art in that they deal with caching write data.

It would have been obvious at the time of the invention to design Hubis' cache system to handle write bursts and cache the write data while forwarding the write command to the drive, as taught by Rowson.

The motivation for doing so, as taught by Rowson, would be to minimize on-drive resources *(section 5, paragraph 6, line 3)* and to allow the drive to read data in an order optimized for disk scheduling *(section 5, paragraph 7, lines 10-12)*.

Therefore, it would have been obvious to combine Hubis and Kitamura's cache system with Rowson's write burst for the benefit of minimizing on drive resources and optimizing disk scheduling to obtain the invention as specified in claim 6.

27.   As per **Claim 14**, Hubis, Kitamura and Rowson disclose the storage control method according to claim 9, further comprising a step of writing *(section 5, paragraph 7 lines 1-4)* the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying when said one controller receives a data write request for a plurality of pages *(write-burst, section 5 paragraph 6 lines 1-3)* from said requesting apparatus.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Li

28.   **Claims 8 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and Kitamura *(US Patent Number 6,247,012)* as applied to claims 7 and 15 respectively above, in further view of Li et al *("Evaluation of Memory System Extensions")*.

29.   As per **Claim 8**, Hubis and Kitamura disclose the storage control apparatus according to claim 7, wherein said first control unit instructs *(Hubis, mirror cache write command, column 3 lines 57-58)* said first node channel circuit to execute the transfer of data of the page allocated in the read/write area of said first cache memory to the acquired page in the mirror area of said second cache memory, and performs said copying *(Hubis, column 3 lines 52-55)*.

Hubis and Kitamura do not disclose the transfer being a DMA transfer.

Li discloses transferring data blocks between memories where the transfer is a DMA transfer *(lines 7-17, paragraph 3 of page 91).*

Hubis, Kitamura and Li are analogous art in that they deal with transferring data between memory elements.

It would have been obvious to one with ordinary skill in the art to utilize DMA transfer when transferring data between the first and second controllers. The motivation for doing so would have been to allow the controller's control unit to do other useful work during the period of transfer *(lines 13-14, paragraph 3 of page 91).*

Therefore, it would have been obvious to combine the transfer of data used in Hubis and Kitamura with the DMA transfer described by Li for the benefit of increased processing time to obtain the invention as specified in claim 8.

30.   As per **Claim 16**, Hubis, Kitamura and Li disclose the storage control method according to claim 15, wherein said copying step comprises a step of said first control unit instructing *(Hubis, mirror cache write command, column 3 lines 57-58)* said first node channel circuit to execute the DMA transfer *(Li, lines 7-17, paragraph 3 of page 91)* of the data of the page allocated in the read/write area of said first cache memory to the acquired page in the mirror area of said second cache memory and performing said copying *(Hubis, column 3 lines 52-55).*

III. **CLOSING COMMENTS**

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

a. **STATUS OF CLAIMS IN THE APPLICATION**

31.   The following is a summary of the treatment and status of all claims in the

application as recommended by M.P.E.P. ' 707.07(i):

a(1). **CLAIMS REJECTED IN THE APPLICATION**

32.   Per the instant office action, Claims 1-16 have received a second action on the

merits and are subject of a final action.

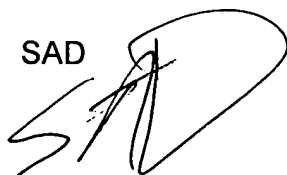## b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 8:30-5:00.
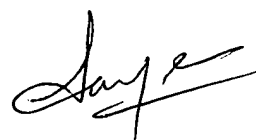
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

SAD

SANJIV SHAH
PRIMARY EXAMINER